Model 2 Klee Mnemonic Table

Mnemonic	Circuits Involved	Description
Bus *n* Gate	Gate Bus	0 to 5V or 0 to 10V (depending on resistor arrangement noted on the Gate Bus schematic) signal. Gate signal that connects to a front panel gate bus output, where *n* signifies if it is to be connected to the Bus 1, Bus 2 or Bus 3 gate output.
Bus *n* LED	Gate Bus	0 to +15V signal that follows the specified output, signified by *n* and is used to drive the corresponding gate bus LED indicator (Bus 1, Bus 2 or Bus 3).
Bus *n* Trig	Gate Bus	0 to 5V or 0 to 10V (depending on resistor arrangement noted on the Gate Bus schematic) 1 ms wide pulse signal. Trigger signal that connects to a front panel gate bus output, where *n* signifies if it is to be connected to the Bus 1, Bus 2 or Bus 3 trigger output.
Bus Ref	Gate Bus	+1.95V reference voltage for gate bus comparators.
Clock	Clock and Load Gate Bus	0 to +15V signal created from external clock input or Manual Step Key. Used to initiate a shift right on positive transition.
Clock In	Clock and Load	External clock input signal from front panel Clock In Jack.
D_Clock	Gate Bus	0 to 15V signal. This is a slightly delayed version of 'Clock'. It is used to delay generation of gate and trigger signals slightly so that they occur after the shift register has totally completed its most recent transition.
Gate Load	Clock and Load Gate Bus	0 to +15V signal from Gate Bus 1. When Bus 1 load switch is closed, a high on this signal will initiate a load of the currently programmed pattern.
Load In	Clock and Load	External load input signal from front panel External Load Jack.
Main Out A	Enhanced Voltage Output	Variable voltage between 0 and 8V. This is the Step Mix A signal presented to the outside world. In the enhanced voltage output circuit, this is the voltage after the slew generator that should be connected to the Main A out connector.

Mnemonic	Circuits Involved	Description
Main Out A+B	Enhanced Voltage Output	Variable voltage between 0 and 15V. Voltage produced by adding the Step Mix A and Step Mix B signals together. In the enhanced voltage output circuit, this is the voltage before the slew generator that should be connected to the A+B Main out connector.
Main Out B	Enhanced Voltage Output	Variable voltage between 0 and 8V. This is the Step Mix B signal presented to the outside world. In the enhanced voltage output circuit, this is the voltage after the slew generator that should be connected to the Main B out connector.
Master Gate	Gate Bus	0 to 5V or 0 to 10V (depending on resistor arrangement noted on the Gate Bus schematic) signal. Gate signal that connects to the front panel gate bus Master Gate output.
Master LED	Gate Bus	0 to +15V signal that follows the Master Gate output and is used to drive the Gate Bus Master LED indicator.
Master Trig	Gate Bus	0 to 5V or 0 to 10V (depending on resistor arrangement noted on the Gate Bus schematic) 1 ms wide pulse signal. Trigger signal that connects to the front panel gate bus Master Trigger output.
Max V	Step Decoder Max Voltage Scaler Opt 1 Max Voltage Scaler Opt 2 Max Voltage Scaler Opt 3	0 to +8V variable signal. This signal is produced on the chosen Max Voltage Scale option and determines the maximum voltage value any of the programming pots can contribute to the voltage output.
Out A	Standard Voltage Output Enhanced Voltage Output	Variable voltage between 0 and 8V. This is the Step Mix A signal presented to the outside world. In the standard voltage output circuit, this is the voltage after the slew generator that should be connected to the A Out connector. In the enhanced voltage output circuit, this is the voltage before the slew generator that should be connected to the A out connector.

Mnemonic	Circuits Involved	Description
Out A+B	Standard Voltage Output Enhanced Voltage Output	Variable voltage between 0 and 15V. Voltage produced by adding the Step Mix A and Step Mix B signals together. In the standard voltage output circuit, this is the voltage after the slew generator that should be connected to the A+B Out connector. In the enhanced voltage output circuit, this is the voltage before the slew generator that should be connected to the A+B out connector.
Out B	Standard Voltage Output Enhanced Voltage Output	Variable voltage between 0 and 8V. This is the Step Mix B signal presented to the outside world. In the standard voltage output circuit, this is the voltage after the slew generator that should be connected to the B Out connector. In the enhanced voltage output circuit, this is the voltage before the slew generator that should be connected to the B out connector.
PSA	Clock and Load Stage Encoder	Narrow 0 to +15V pulse used to switch CD4034 Shift Registers to parallel input mode. Goes high before R Async goes high, goes low after R Async goes low.
R Async	Clock and Load Stage Encoder	Narrow 0 to +15V pulse used to switch CD4034 Shift Registers to asynchronous mode so they will load the current bit pattern, which is programmed by the pattern switches.
R Clock	Clock and Load Stage Encoder	0 to +15 V narrow pulse derived from Clock signal, used to clock the shift registers.
Rand In	Stage Encoder	External random input signal from front panel Random In Jack.
Step Mix A	Step Decoder Standard Voltage Output	Variable voltage between 0 and 8V. Voltage produced by the programming pots 1 through 8.
Step Mix B	Step Decoder Standard Voltage Output	Variable voltage between 0 and 8V. Voltage produced by the programming pots 9 through 16.

Mnemonic	Circuits Involved	Description
Step *n*	Stage Encoder Step Decoder Gate Bus	0 to +15V level. The Step *n* signals each represent an individual shift register bit, where *n* is the number corresponding to the associated shift register bit, starting with 1 at left. When the associated bit is low, the Step *n* signal is 0V. When the associated bit is high, the Step *n* signal is +15V.
Switch *n*	Clock and Load Stage Encoder	0 to +15V level. Where *n* is the switch corresponding to the associated pattern bit, starting with 1 at left. When pattern switch *n* is open, the corresponding Switch *n* signal is high. When pattern switch *n* is closed, the corresponding Switch *n* signal is low. These signals are applied to the parallel load input of the CD4034 Shift Register ICs.