Possible SymplSeq (hexinverter) Master & Slave wiring

The diagram below shows the modifications to the logic board that have to be made.
1st you have to cut the “clock trace” that connects the internal clock to IC2/pin14. It would be favourable to do this at the left edge of the board, sonce we could utilize the CLK.A pads as internal clock outputs, and the CLK.B wirepad as clock input.
2nd you have to move R1. This is the pulldown resistor for the 4017’s clock input. R1 has to go from IC2/pin14 to GND.

The diagram to the right shows a possible wiring of one master and 3 slave symplseq’s, using switching sockets and toggles. In any case it would be good to add protecion diodes and propbably an input impedance to the external inputs (CLK.B). If you add an inputimpedance you might have to increase R1 (up to 1M?), since your input impedance and R1 will work as voltage divider.